library ieee;

use ieee.std\_logic\_1164.all;

entity mux is

port(

a: in std\_logic\_vector(7 downto 0);

b: in std\_logic\_vector(7 downto 0);

sel: in std\_logic;

output: out std\_logic\_vector(7 downto 0)

) ;

end mux;

architecture logic of mux is

begin

process(A,B,sel)

begin

if (sel = '0') then

output <= a;

else

output <= b;

end if;

end process;

end logic;